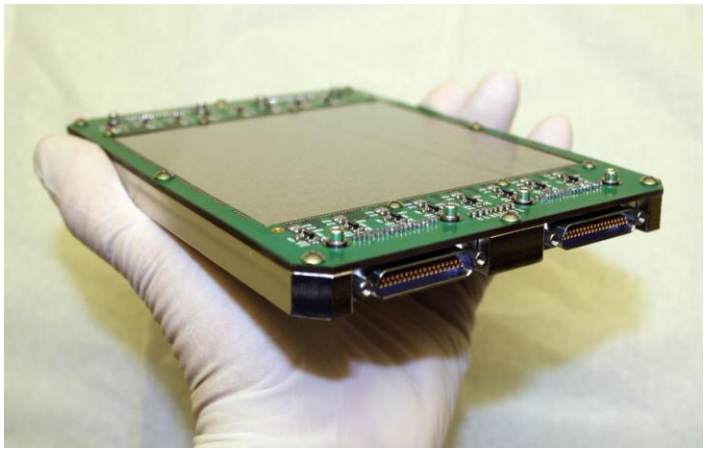
SEMICONDUCTOR TECHNOLOGY ASSOCIATES, Inc

STA1600LN

10560 x 10560 Element Image Area CCD Image Sensor

FEATURES

- 10560 x 10560 Photosite Full Frame CCD Array
- 9 μm x 9 μm Pixel
- 95.04mm x 95.04mm Image Area
- 100% Fill Factor
- Readout Noise 2e- at 50kHz and 5e- at 1MHz
- Dynamic Range > 80dB
- 16 Single Stage Source Follower Output Channels
- Three-Phase Buried Channel NMOS Image area
- Three-Phase Buried Channel Readout Registers
- Multi-Pinned Phase (MPP) optional
- Circular Package Design Option (See appendix A)



GENERAL DESCRIPTION

The STA1600LN is a 10560 x 10560 image element solid state Charge Coupled Device (CCD) Full Frame sensor. This CCD is intended for use in high-resolution scientific, space based, industrial, and commercial electro-optical systems. The STA1600LN is organized in two halves each containing an array of 10560 horizontal by 5280 vertical photosites. The pixel spacing is 9μm x 9μm. For dark reference, each readout line is preceded by 10 dark pixels. This imager is available in a full frame transfer configuration (shown) or a split frame transfer configuration with shield metalization covering half of the imager. The split frame transfer architecture allows higher frame rate operation through four readout quadrants, whereas the single-sided approach allows readout through two readout quadrants. The STA1600LN is offered as a backside illuminated version for increased sensitivity and UV response in the same package configuration.

FUNCTIONAL DESCRIPTION

Image Sensing Elements: Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photoelectrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

The photosite structure is made up of contiguous CCD elements with no voids or inactive areas. In addition to sensing light, these elements are used to shift image data vertically. Consequently, the device needs to be shuttered during readout.

Vertical Charge Shifting: The Full Frame architecture of the STA1600LN provides video information as a single sequential readout of 5280 lines containing 1320 photosites. At the end of an integration period the ϕA_1, ϕA_2, and ϕA_3 clocks are used to transfer charge vertically through the CCD array to the horizontal readout register. Vertical columns are separated by a channel stop region to prevent charge migration.

The imaging area is divided into an Upper and Lower half. Each 10560 x 5280 half may be clocked independently or together. The eight horizontal serial registers along the top and bottom permit simultaneous readout of both halves. The STA1600LN may be clocked such that the full array is readout by the Upper or Lower eight serial registers.

Serial Charge Transfer: ϕS_1, ϕS_2 and ϕS_3 are polysilicon gates used to transfer charge horizontally to the output amplifiers. The horizontal serial register is twice the size of the photosite to allow for vertical binning. For both frame transfer configurations, the charge may be read out through the eight amplifiers at the bottom or top of the image area.

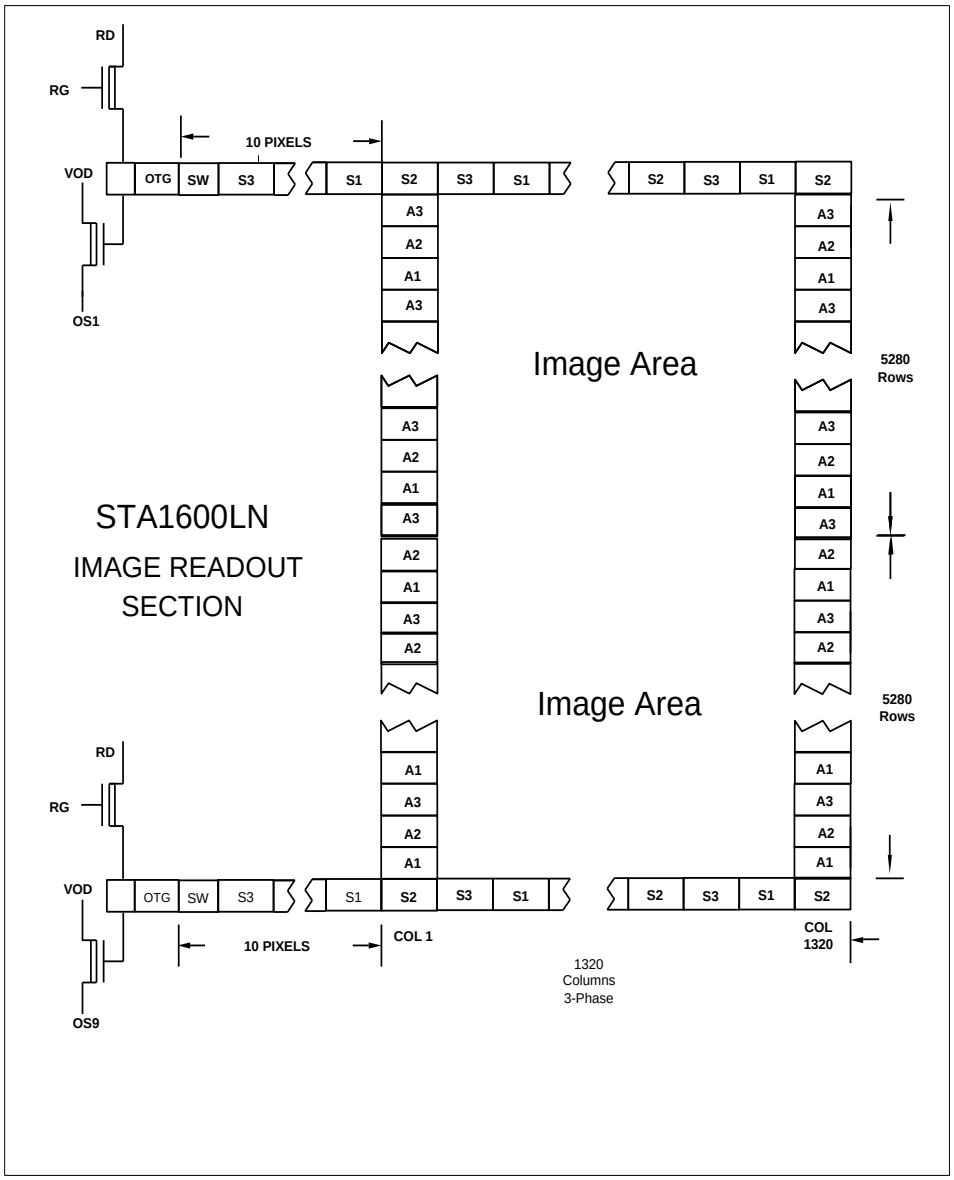
The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 10 additional register cells between the first pixel of each line and the output amplifier. The output from these locations contains no signal and may be used as a dark level reference.

The last clocked gate in the Horizontal registers (ϕSW) is twice as large as the others and can be used to horizontally bin charge. This gate requires its own clock, which may be tied to ϕH_2 for normal full resolution readout.
The reset FET in the horizontal readout, clocked appropriately with ϕRG, allows binning of adjacent pixels in the sense node.

Output Amplifier: The STA1600LN has 16 output amplifiers, one at the end of each Horizontal register section. They are low noise single stage FET floating diffusion amplifiers with a reset MOSFET tied to the input gate.
The output capacitor is reset via the reset MOSFET with ϕRG to a pre-charge level prior to the arrival of the next charge packet except when horizontally binning.
The output amplifier drains are tied to OD. The source is connected to an external load resistor to ground and constitutes the video output from the device
Charge packets are clocked to a pre-charged capacitor whose potential changes linearly in response to the number of electrons delivered. When this potential is applied to the input gate of an NMOS amplifier, a signal at the output V_{out} pin is produced.

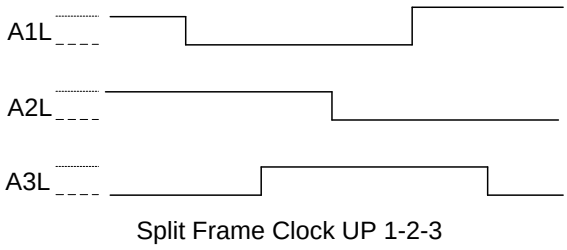
Variants: The STA1600LN can be configured as a multi-pinned phase device. The only deviation from standard operation in that the vertical phases remain off during integration. The backside illuminated STA1600LN is available in standard and deep depletion configurations. The AR coatings can be tuned to meet the customer's needs. The STA1600LN can be configured in a buttable package allowing for less than 12mm of space between active pixel regions.

STA1600LN Gate Configuration

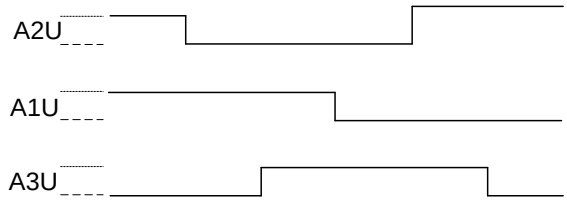


STANDARD CCD TIMING

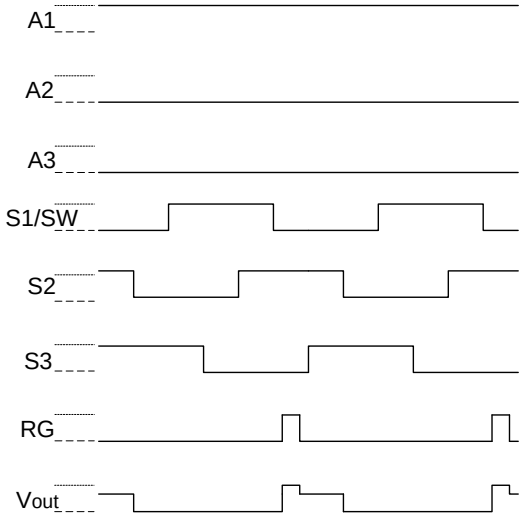
STA1600LN Timing Diagrams



Split Frame Clock UP 1-2-3



Split Frame Clock Down 2-1-3



Serial Readout 1-2-3

DEFINITION OF TERMS

Charge-Coupled Device A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Vertical Transport Clocks ϕA_1, ϕA_2, ϕA_3 the clock signals applied to the vertical transport register.

Horizontal Transport Clocks ϕS_1, ϕS_2, ϕS_3 the clock signals applied to the horizontal transport registers.

Reset Clock ϕRG the clock applied to the reset switch of the output amplifier.

Dynamic Range The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

Saturation Exposure The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Responsivity The output signal voltage per unit of exposure.

Spectral Response Range The spectral band over which the response per unit of radiant power is more than 10% of the peak response.

Photo-Response Non-Uniformity The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.
Dark Signal The output signal is caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

Vertical Transfer Gate ϕVTG Gate structures adjacent to the end row of photosites and the horizontal transport registers. The charge packets accumulated in the photosites are shifted vertically through the array. Upon reaching the end row of photosites, the charge is transferred in parallel via the transfer gates to the horizontal transport shift registers whenever the transfer gate voltage goes low.

Pixel Picture element or sensor element, also called photo element or photosite

DC OPERATING CHARACTERISTICS						
SYMBOL	PARAMETER	RANGE MIN	NOM	MAX	UNIT	REMARKS
V_{OD}	DC Supply Voltage		+25.0		V	
V_{RD}	Reset Drain Voltage		16.0		V	
V_{OTG}	Output Voltage	-2.0	1.0	2.0	V	
V_{SC}	Scupper Voltage		+20.0		V	
V_{SUB}	Substrate Ground		0.0		V	
V_{P_High}	Preamp High Voltage		5.0		V	Powers Output Buffer (P5V)
V_{P_Low}	Preamp Low Voltage		-5.0		V	Powers Output Buffer (N5V)

TYPICAL CLOCK VOLTAGES					
SYMBOL	PARAMETER	HIGH	LOW	UNIT	REMARKS
$V\phi_{S(1,2,3)}$	Horizontal Multiplexer Clock	+5.0	-5.0	V	Note 1
$V\phi_{SW}$	Summing Gate Clock	+5.0	-5.0	V	Note 1
$V\phi_{V(1,2,3)}$	Vertical Array Clocks	+3.0	-9.0	V	Note 1
$V\phi_{RG}$	Reset Array Clock	+5.0	-5.0	V	Note 1

Note 1: ϕH = 200pF, ϕV = 15,000pF. All clock rise and fall times should be > 10 ns.

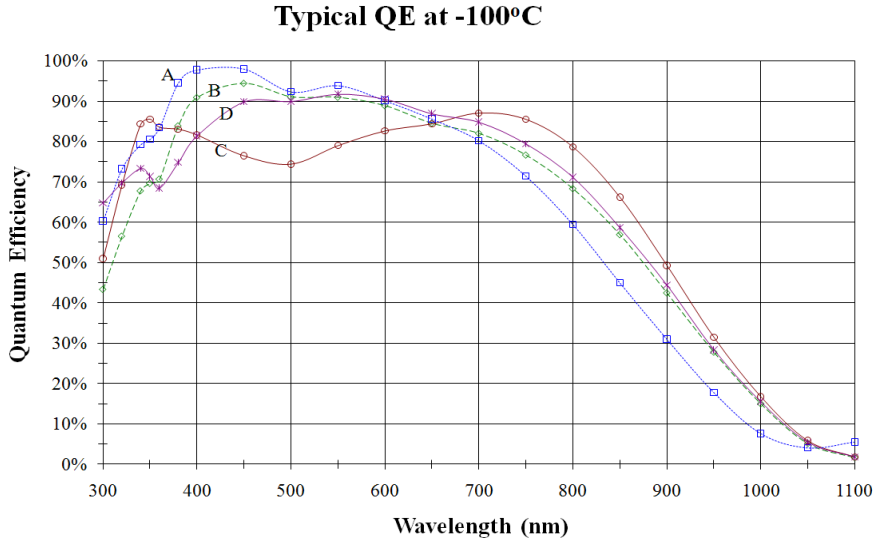
AC CHARACTERISTICS Standard test conditions are nominal clocks and DC operating Voltages, 100 kH_z Horizontal Data Rate,10µSec Vertical shift cycle

SYMBOL	PARAMETER	RANGE MIN	NOM	MAX	UNIT	REMARKS
V_{ODC}	Output DC Level		16.0		V	
Z	Suggested Load Register	1.0	5.0	20.0	kΩ	

PERFORMANCE SPECIFICATIONS						
SYMBOL	PARAMETER	RANGE MIN	NOM	MAX	UNIT	REMARKS
V_{SAT}	Saturation Output Voltage Full Well Capacity Output Amp Sensitivity		700 70K 80K 7.0	100K	mV e- µV/e-	Note 1
PRNU	Photo Response Non- Uniformity Peak-to-Peak		10		$\%V_{SAT}$	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak		1.0		mV	
DC	Dark Current		3.0	5.0	e-/pix/hour	@ -100C
rms	Noise		2.5	4.0	e-	@ 100 kHz
			5.0	7.0	e-	@ 1Mhz

Note 1: Maximum well capacity is achieved in Buried Channel Mode.

QUANTUM EFFICIENCY ENHANCEMENTS



The STA1600LN CCD area arrays can be backside thinned for increased QE. The incident illumination enters through the backside of the array, Devices can be supplied with tailored AR coatings for optimized peak quantum efficiency.

COSMETIC GRADING

Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels, and for different device temperatures.

The STA1600LN is available in various standard grades, as well as custom selected grades. Consult Semiconductor Technology Associates for available grading information and custom selections.

COSMETIC GRADING								
	Specifications				**Typical Values**			
Grade	A	B	C	ENG_1	A	B	C	ENG_1
Column Defects	10	20	30	>30	0	<5	<10	>15
Hot Pixels	1000	2000	3000	>3000	<500	<100	<900	>1500
Dark Pixels	400	800	1000	>1000	<300	<700	<800	>1000
Traps > 200e-	20	30	40	>40	<5	<10	<25	>40

1. Engineering Grade devices will typically have 1 or more non-functioning outputs

Definitions	
Column Defect	Column with >20 contiguous hot or dark pixels, or column containing >10% gain variation from adjacent columns.
Hot Pixels	A hot pixel is defined as a pixel with dark current generation of 5e-/pixel/sec at -100^{o}C.
Dark Pixels	A dark pixel is defined as a pixel with photo-response less than 50% of the local mean.
Traps	A trap is defined as a pixel that temporarily holds charge at a value greater than 200e-.

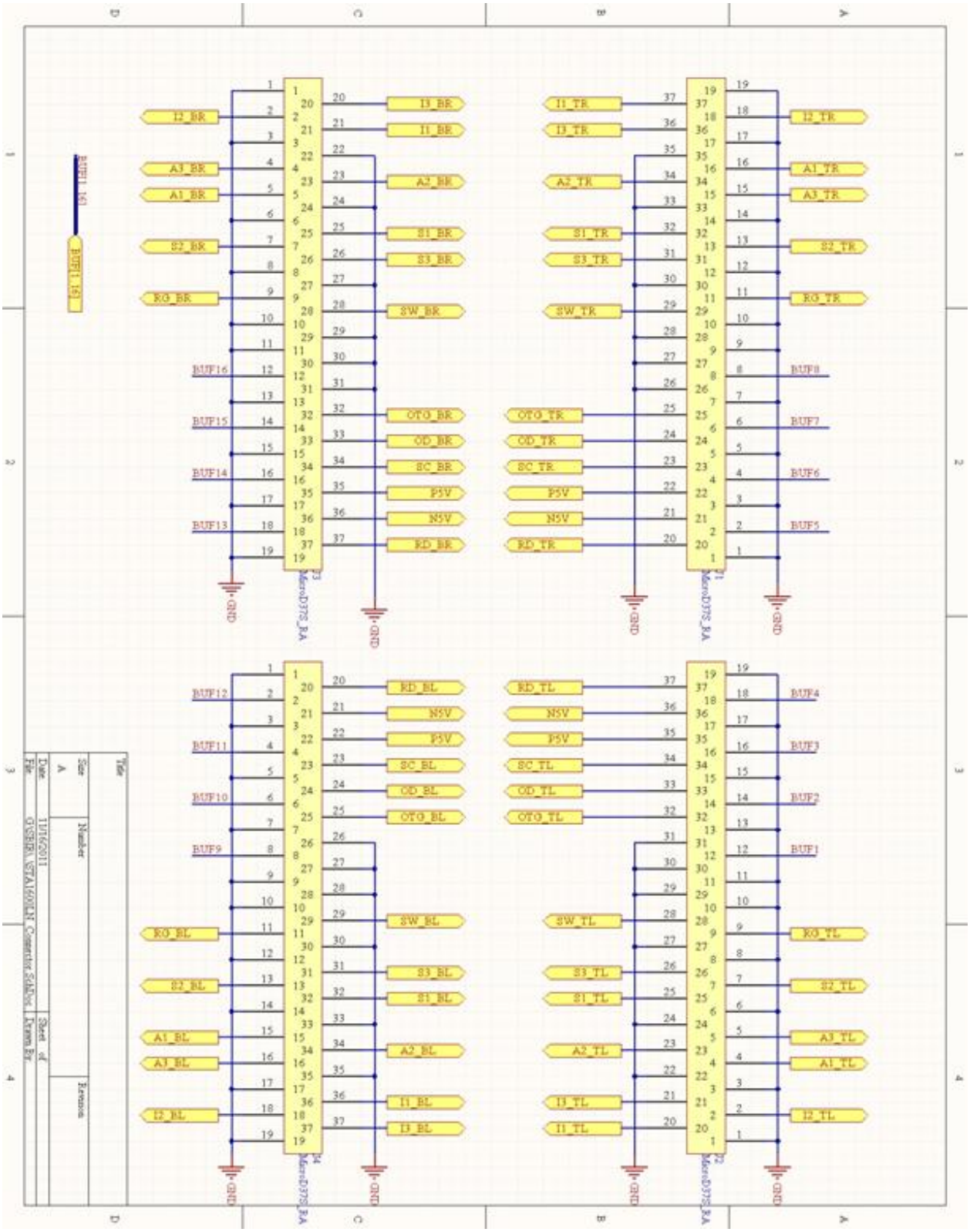
WARRANTY

Within twelve months of delivery to the end customer Semiconductor Technology Associates will repair or replace, at our option, any image sensor product if any part is found to be defective in materials or workmanship. Contact Semiconductor Technology Associates for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

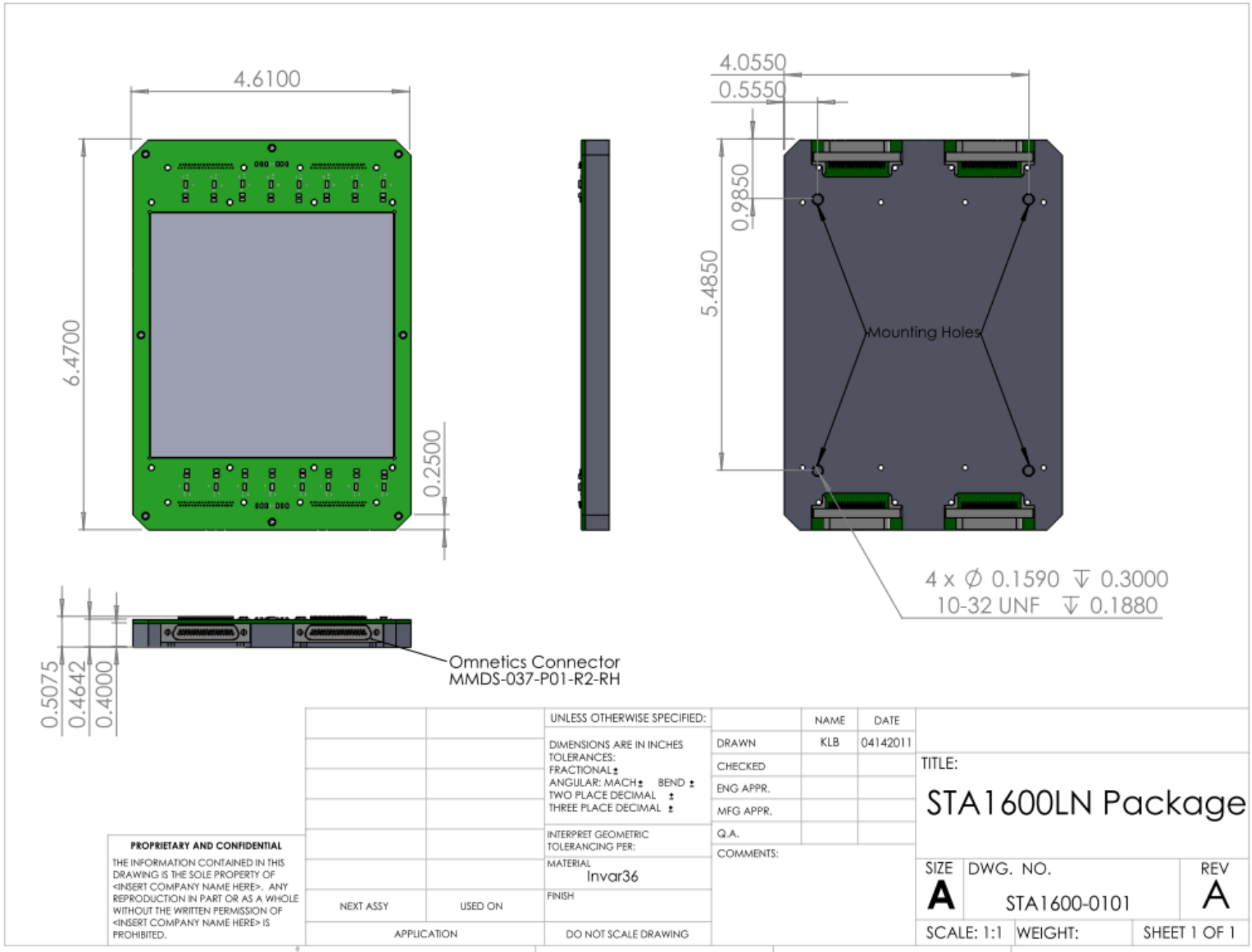
CERTIFICATION

Semiconductor Technology Associates certifies that all products are carefully inspected and tested prior to shipment and will meet all of the specification requirements under which it is furnished

STA1600LN Image Sensor Connector Pin Designation



Note: Vertical Image sections are designated as A1,A2,A3 and I1, I2, I3 clocking for each is identical unless running in a split frame transfer configuration.



		UNLESS OTHERWISE SPECIFIED:		NAME	DATE
		DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONAL ± ANGULAR: MACH ± BEND ± TWO PLACE DECIMAL ± THREE PLACE DECIMAL ±	DRAWN	KLB	04142011
			CHECKED		
			ENG APPR.		
			MFG APPR.		
		INTERPRET GEOMETRIC TOLERANCING PER:	Q.A.		
		MATERIAL Invar36	COMMENTS:		
NEXT ASSY	USED ON	FINISH			
APPLICATION		DO NOT SCALE DRAWING			

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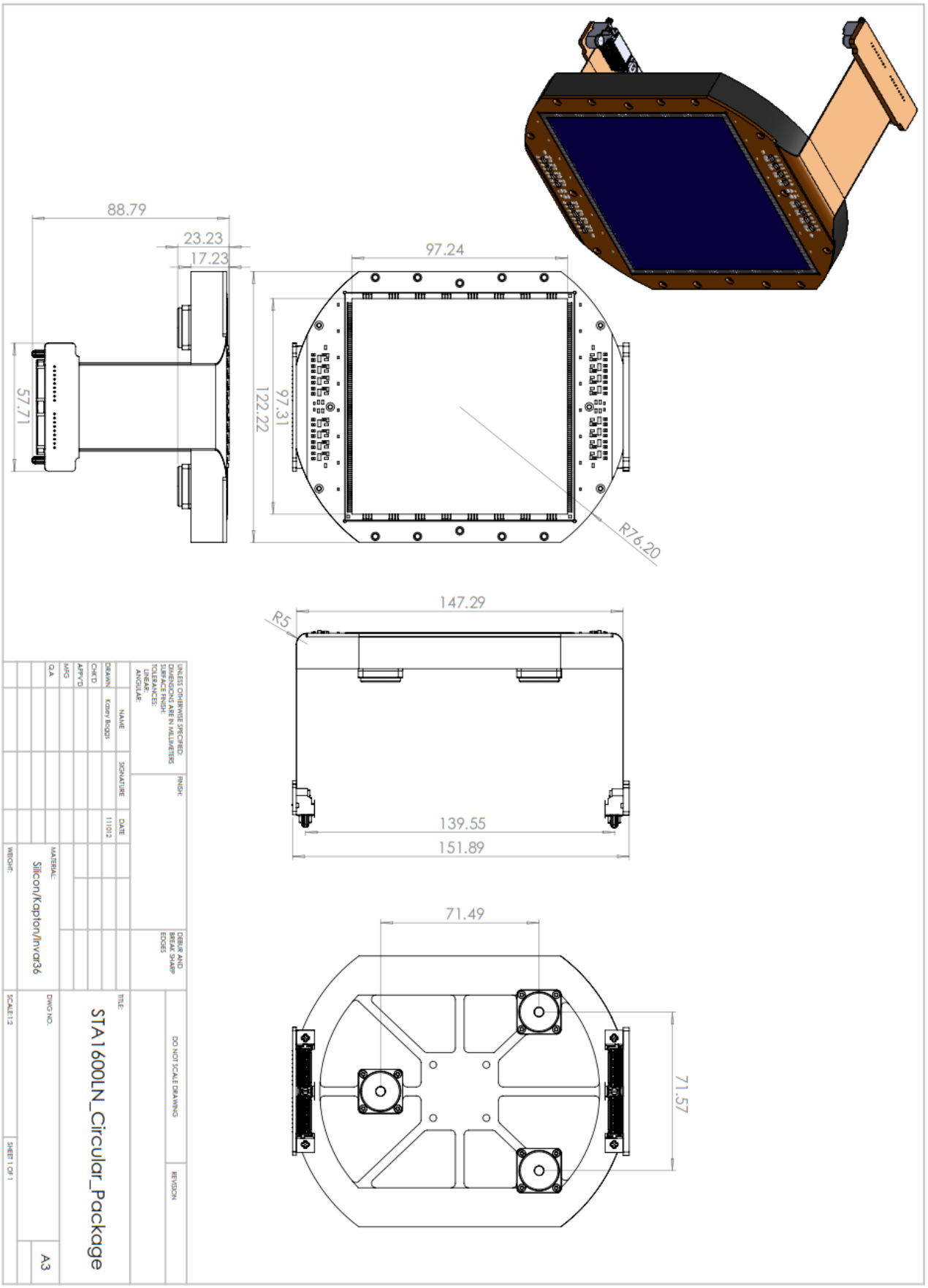
TITLE:

STA1600LN Package

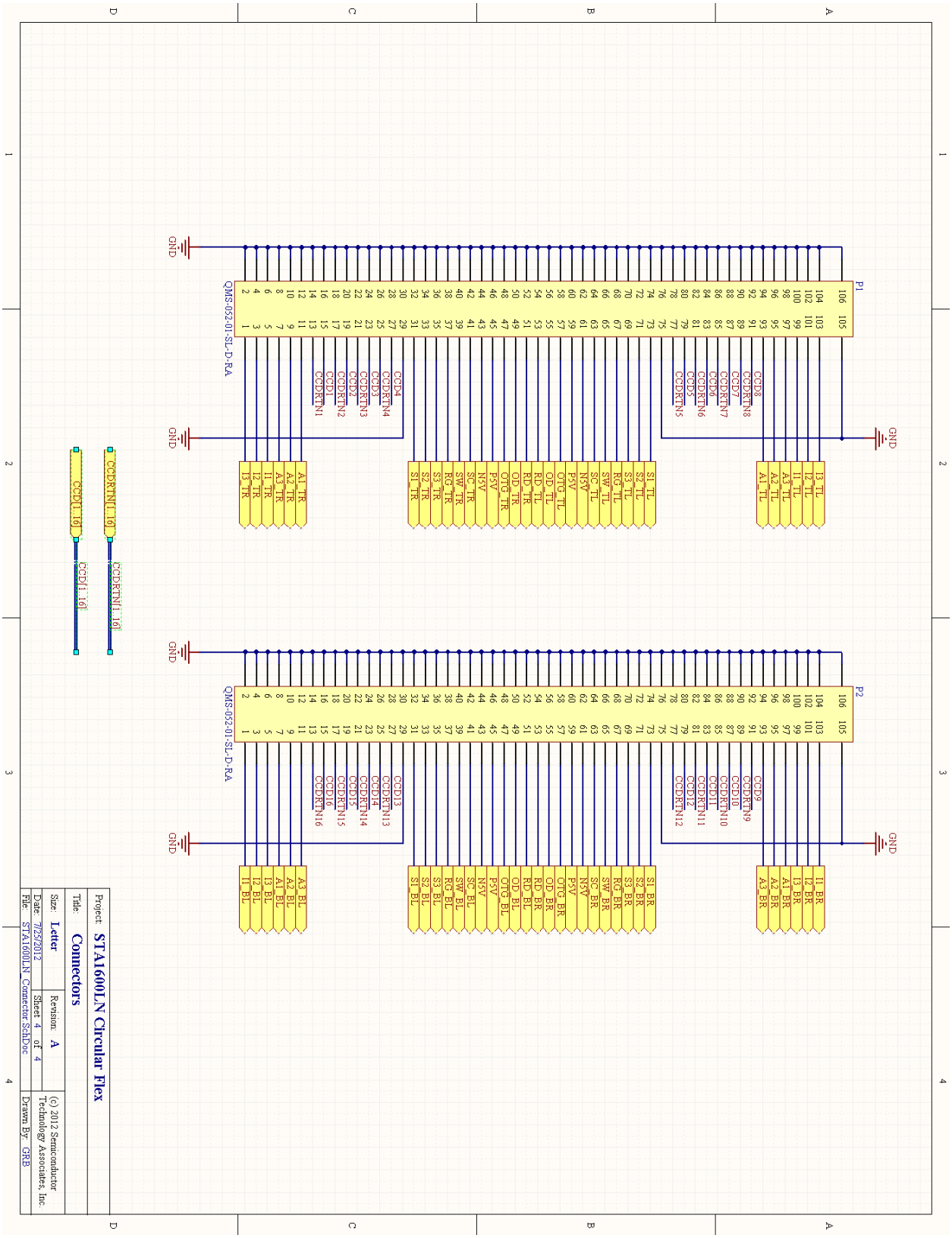
SIZE	DWG. NO.	REV
A	STA1600-0101	A
SCALE: 1:1	WEIGHT:	SHEET 1 OF 1

5 4 3 2 1

APPENDIX A: STA1600LNC Circular Package Option



STA1600LNC Image Sensor Connector Pin Designation



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