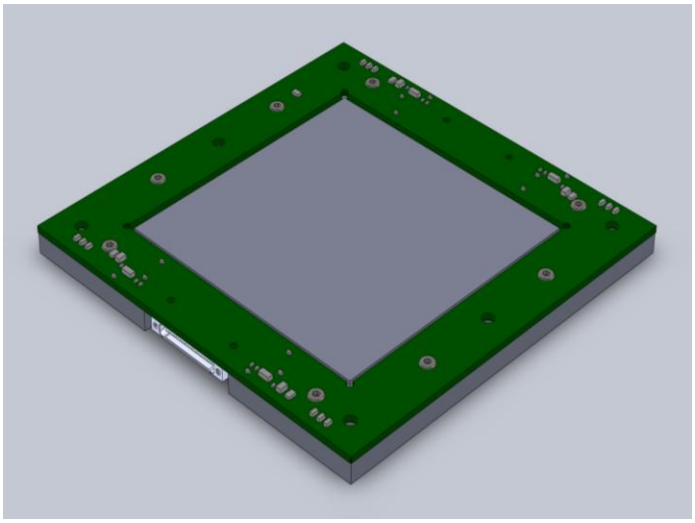
SEMICONDUCTOR TECHNOLOGY ASSOCIATES, Inc

STA4150A

4096 x 4096 Element Image Area CCD Image Sensor

FEATURES

- 4096 x 4096 CCD Image Array
- 15 μm x 15 μm Pixel
- 61.44mm x 61.44mm Image Area
- Near 100% Fill Factor
- Readout Noise Less Than 3 Electrons at 100KHz
- 4 Single Stage 3MHz Outputs
- Three-Phase Buried Channel Image area
- Multi-pinned Phase (MPP)
- Three-Phase Buried Channel Readout Registers
- Selectable Video Output Channels
- Backside Illuminated



GENERAL DESCRIPTION

The STA4150A is a 4096 x 4096 image element solid state Charge Coupled Device CCD sensor. This CCD is intended for use in high-resolution scientific, space based, industrial, and commercial electro-optical systems. The STA4150A is organized in two halves each containing an array of 4096 horizontal by 2048 vertical photosites. The STA4150A may be operated in either buried-channel or MPP mode. The pixel spacing is 15μm x 15μm. For dark reference, each readout line is preceded by 4 extended pixels. The single stage output architecture allows low noise operation through four readout sections. The STA4150A is offered as a backside illuminated version for increased sensitivity and UV response in the same package configuration.

FUNCTIONAL DESCRIPTION

Image Sensing Elements: Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. During integration, the collected photoelectrons are related directly to the amount of charge accumulated at each pixel. There is a linear relationship between the incident illumination intensity and the integration time.

The photosite structure is made up of a series of closely spaced MOS capacitors elements. These photosites sense light, then shift the light vertically via potential wells created by the vertical array clocks.

Vertical Charge Transfer: The charge may be shifted in one of three methods, split frame transfer to outputs 1,2,3 and 4, single frame transfer to outputs 1 or 2, or single frame transfer to outputs 3 or 4. At the end of an integration period the A1, A2, and A3 clocks are used to transfer charge vertically through the CCD array to the horizontal

readout registers. Vertical columns are separated by a channel stop region to prevent charge migration

The imaging area is divided into an Upper and Lower halves. Each 4096 x 2048 section may be clocked independently or together. Horizontal serial registers along the top and bottom permit simultaneous readout of both halves. The STA4150A may be clocked such that the full array is readout by the upper or lower serial registers.

Serial, Charge Transfer: S1, S2 and S3 are polysilicon gates used to transfer charge horizontally to the output amplifiers. The horizontal serial register is twice the size of the photosite to allow for vertical binning. For both frame transfer configurations, the charge may be read out through the amplifiers at the bottom or top of the image area.

The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 4 additional register cells between the first pixel of each line and the output amplifier. The output from these locations contains no signal and may be used as a dark level reference

The last clocked gate in the Horizontal registers is twice as large as the others and can be used to horizontally bin charge. This gate requires its own clock, which may be tied to the next ordered serial clock for normal full resolution readout.

The reset FET in the horizontal readout, clocked appropriately with RG, allows binning of adjacent pixels.

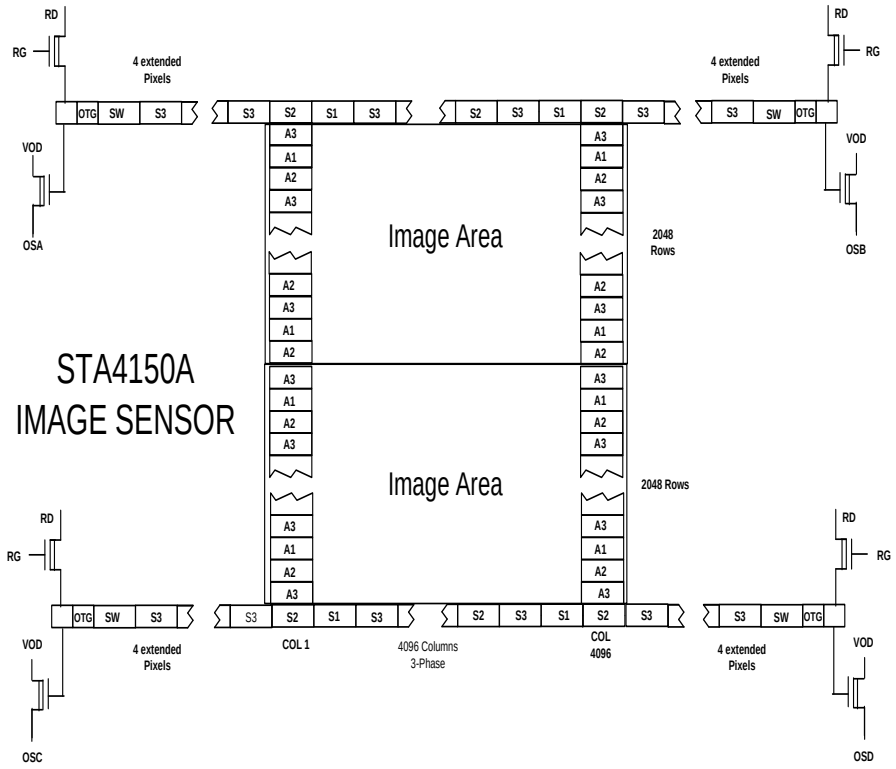
Output Amplifier: The STA4150A has four single stage source followers that have proven low noise performance at the end of each Horizontal register.

The output capacitor is reset via the reset MOSFET with ϕRG to a pre-charge level prior to the arrival of the next charge packet except when horizontally binning.

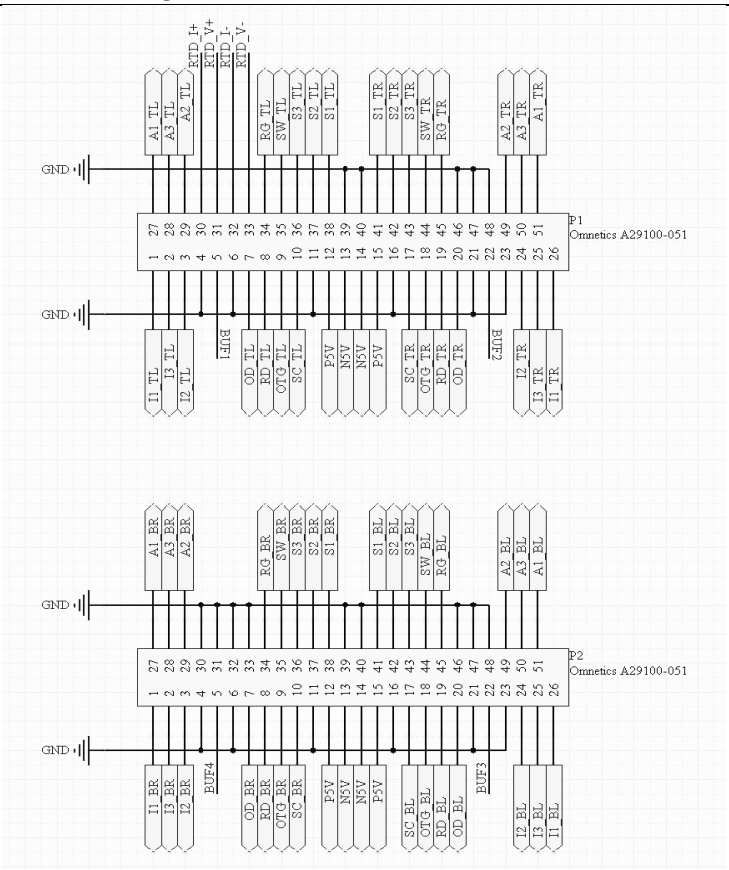
The output amplifier drains are tied to OD. The source is connected to an external load resistor to ground and constitutes the video output from the device

Charge packets are clocked to a pre-charged capacitor whose potential changes linearly in response to the number of electrons delivered. When this potential is applied to the input gate of an NMOS amplifier, a signal at the output V_{out} pin is produced.

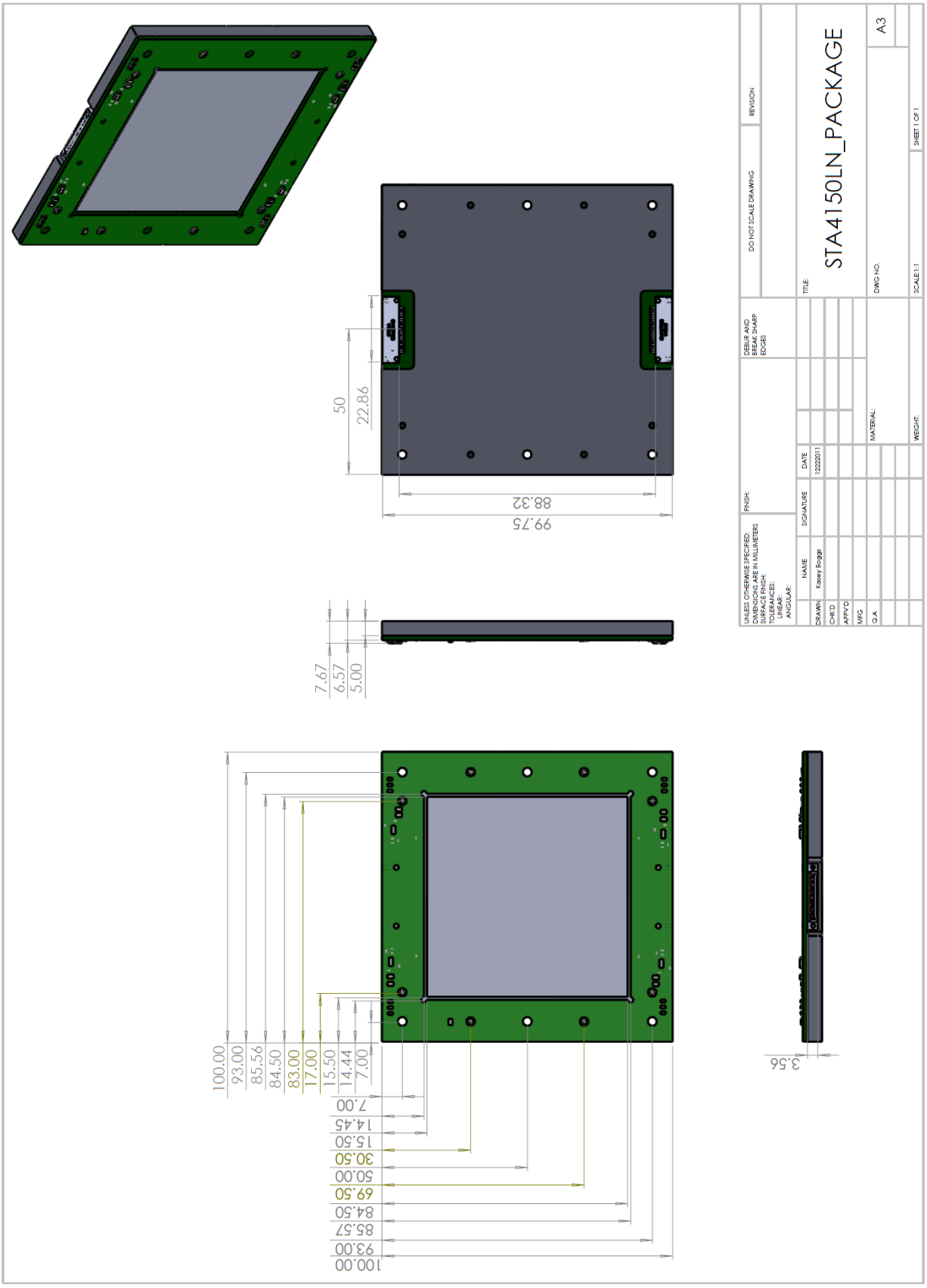
STA4150A Gate Configuration



STA4150A Connector Configuration

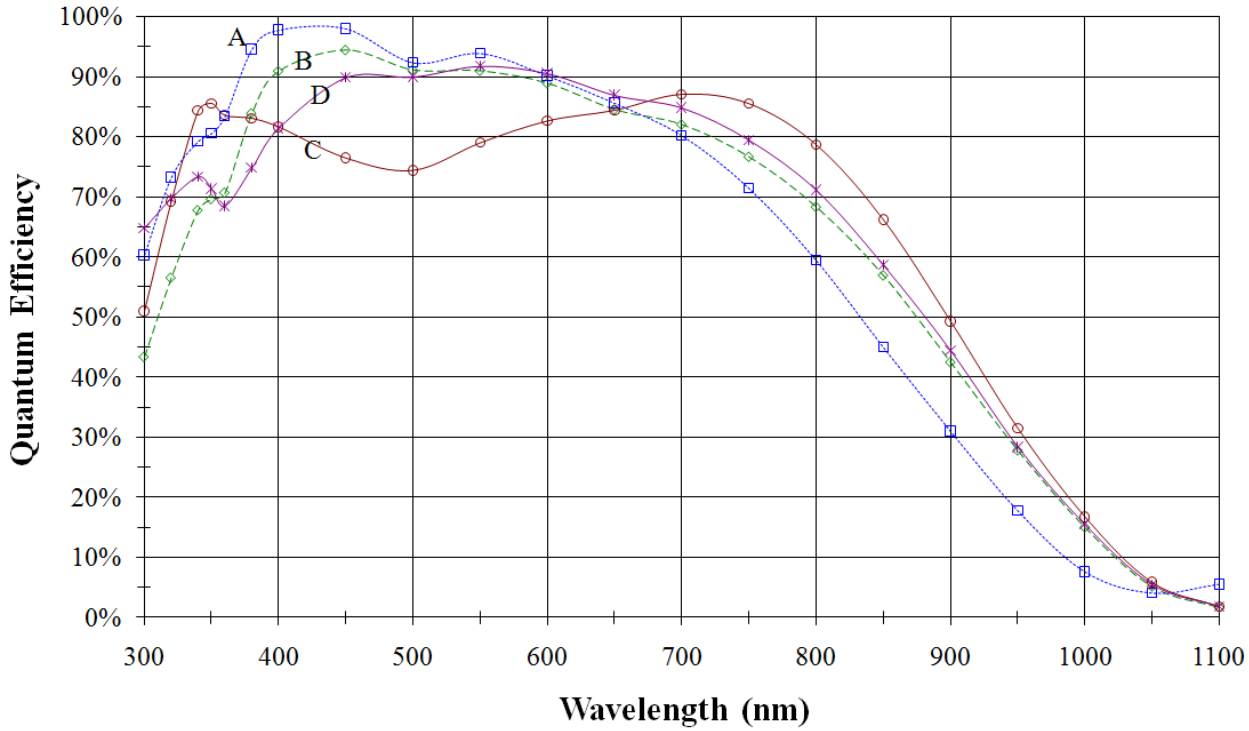


STA4150A Package Configuration

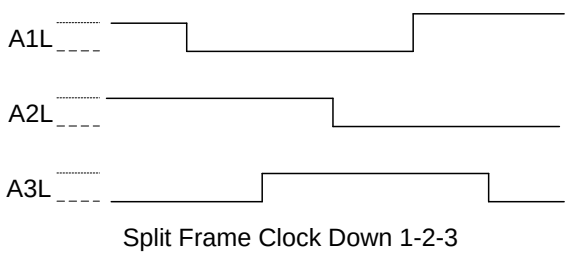


DC OPERATING CHARACTERISTICS						
SYMBOL	PARAMETER	RANGE MIN	NOM	MAX	UNIT	REMARKS
OD	DC Supply Voltage	15.0	24.0	30.0	V	
RD	Reset Drain Voltage	10.0	15.0	20.0	V	
OTG	Output Transfer Gate Voltage	-5.0	-1.0	5.0	V	
Vss	Substrate Ground	0.0			V	
TYPICAL CLOCK VOLTAGES						
SYMBOL	PARAMETER	HIGH		LOW	UNIT	REMARKS
S1,S2,S3	Horizontal Serial Clocks	+5.0		-5.0	V	Typical clock range
SW	Summing Gate Clock	+5.0		-5.0	V	Clock as S1 clocked separately
A1,A2,A3	Vertical Array Clocks	+3.0		-9.0	V	
RG	Reset Gate Array Clock	+8.0		-2.0	V	
AC CHARACTERISTICS						
SYMBOL	PARAMETER	RANGE MIN	NOM	MAX	UNIT	REMARKS
V_{ODC}	Output DC Level		16.0		V	Typical
Zsingle	Suggested Load Resistor	3.0	10.0	20.0	kΩ	Higher resistance reduces bandwidth
PERFORMANCE SPECIFICATIONS						
SYMBOL	PARAMETER	RANGE MIN	NOM	MAX	UNIT	REMARKS
V_{SAT} FWC (Image) FWC(SW)	Saturation Output Voltage Full Well Capacity	700 150k	200k TBD		mV e-	
	Output amplifier sensitivity	4.0	5.0		μV/e-	
PRNU	Photo Response Non-Uniformity Peak-to-Peak			10	$\%V_{SAT}$	
CTE	Charge Transfer Efficiency	>0.99999				
DC	Dark Current		3.0	5.0	e-/pix/hour	$-110^{O}C$
	Output Linearity	< 2%				Full Scale
N_{RMS}	Readout Noise		2	4	e-	100KHz

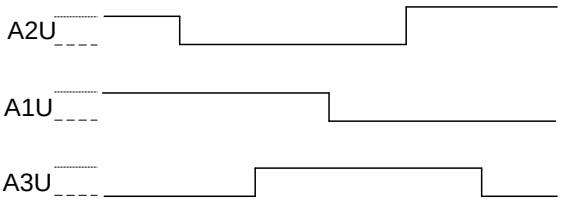
Typical QE at -100°C



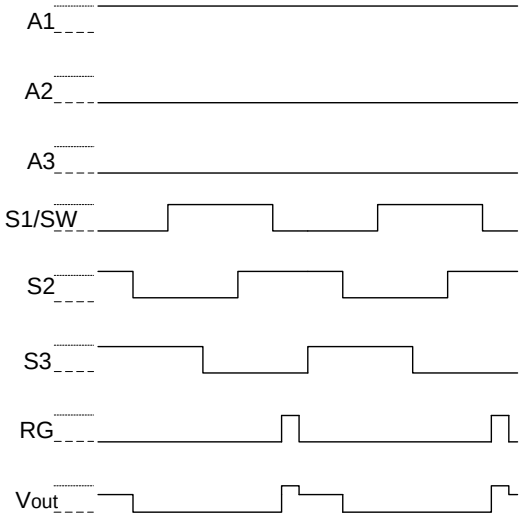
STA4150A Timing Diagrams



Split Frame Clock Down 1-2-3



Split Frame Clock Up 2-1-3



Serial Readout 1-2-3

COSMETIC GRADING

The STA4150A CCD image sensor is available in various standard grades, as well as custom grades. Consult Semiconductor Technology Associates for further information on grade selection.

COSMETIC GRADING								
	Specifications				Typical Values			
Grade	A	B	C	ENG_1	A	B	C	ENG_1
Column Defects	5	10	15	>15	0	<5	<10	>15
Hot Pixels	500	800	1500	>1500	<300	<500	<1000	>1500
Dark Pixels	400	800	1000	>1000	<200	<700	<800	>1000
Traps > 200e-	10	15	20	>20	<5	<10	<15	>20

1. Engineering Grade devices will typically have 1 or more non-functioning outputs

Definitions	
Column Defect	Column with >20 contiguous hot or dark pixels, or column containing >10% gain variation from adjacent columns.
Hot Pixels	A hot pixel is defined as a pixel with dark current generation of 5e-/pixel/sec at -100^{o}C.
Dark Pixels	A dark pixel is defined as a pixel with photo-response less than 50% of the local mean.
Traps	A trap is defined as a pixel that temporarily holds charge at a value greater than 200e-.

WARRANTY

Semiconductor Technology Associates will repair or replace, at our option, any image sensor product within twelve months of delivery to the end customer, for any defect in materials or workmanship. Contact Semiconductor Technology Associates for further warranty information, a return number, and shipping instructions

CERTIFICATION

Semiconductor Technology Associates certifies that all products are carefully inspected and tested prior to shipment and will meet all of the specification requirements under the performance specifications summarized.